Customer No.: 31561
Application No.: 10/710,729
Docket No.: 13135-US-PA

REMARKS

Present Status of the Application

The Office Action rejected claims 1-6, 8-9 under 35 U.S.C. 103(a), as being unpatentable over Han (U.S. 2003/0155572 A1). The Office Action rejected claim 8 under 35 U.S.C. 103(a) as being unpatentable over Han in view of Sun (U.S. 6,936,848). The Office Action also rejected claim 9 under 35 U.S.C. 103(a) as being unpatentable over Han in view of Peng (U.S. 6,835,606).

Applicant has amended claim 1 to more clearly define the present invention. The limitation added in claim 1 is shown in Figs. 4A-4B and described in paragraphs [0039]-[0041], and no new matter is entered. After entry of the foregoing amendments, claims 1-6 and 8-9 remain pending in the present application, and reconsideration of those claims is respectfully requested.

Discussion of Office Action Rejections

Applicant respectfully traverses the 103(a) rejection of claims 1-6, 8-9 as being unpatentable over Han (U.S. 2003/0155572 A1)because a prima facie case of obviousness has not been established by the Office Action.

> To establish a prima facie case of obviousness under 35 U.S.C. 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three

requirements must " be found in the prior art, and not be based on applicant's disclosure." See M.P.E.P. 2143, 8th ed., February 2003.

The present invention is in general related a low temperature polysilicon thin film transistor (LTPS-TFT) structure as claim 1 recites:

Claim 1. A low temperature polysilicon thin film transistor (LTPS-TFT) structure disposed on a substrate, comprising:

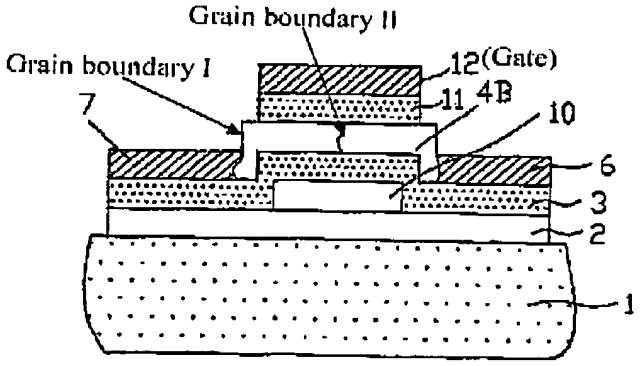
a cap layer disposed over the substrate, wherein there is a gap between the cap layer and the substrate;

a polysilicon film disposed over the cap layer, wherein the polysilicon film comprises a channel region and a source/drain region on each side of the channel region, and the channel region is directly above the gap; and

a gate disposed above the channel region of the polysilicon film, ***wherein the width of the gate is smaller than the average grain size of the channel region, and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate.***

Han fails to disclose, teach or suggest the width of the gate is smaller than the average grain size of the channel region, and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate. Han discloses a thin film transistor, as shown in Fig. 5D, including a buffer layer 2, an oxide layer 3, an air gap 10, a polysilicon layer 4B (channel), a source 6, a drain 7, a gate oxide layer 11 and a gate 12. In particular, the air gap 10 is provided to reduce heat transmission along a vertical direction. The solicidation at the channel proceeds towards the center of the channel from the boundaries between the channel region and the drain and source regions (paragraph [0024]). Thus, grains of the channel laterally grow to fully fill out the active layer of the channel from the boundaries towards the center of the channel. However, Han does not teach or suggest that the gate has a width smaller than the average grain

size of the channel region, and ***the gate does not cross the grain boundary*** in a direction parallel to the extension direction of the gate. Han just discloses forming an aluminum layer 12 as a gate electrode, but Han does not describe about the width of the gate electrode and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate. As a matter of fact, in Fig. 5D of the Han reference, the gate 12 crosses the grain boundary II.



In claim 1 of the present application, the gate has a width smaller than the average grain size of the channel region and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate. Therefore, the channel region of the thin film transistor is prevented from crossing the grain boundary so that the thin film transistor can have a better performance. In addition, if the gate is a dual gate structure as recited in claim 8, the effect of the grain boundary in the middle of the channel on the electrons is substantially reduced so that the transistor can have a much better performance.

The office action stated Han does not explicitly teach that the width of the gate is 10 um in Figs. 6-7. However, applicant disagrees. Han teaches W/L=10um/8.7um in Figs. 6-7. One skilled in the art understands W of W/L means the gate width or channel width.

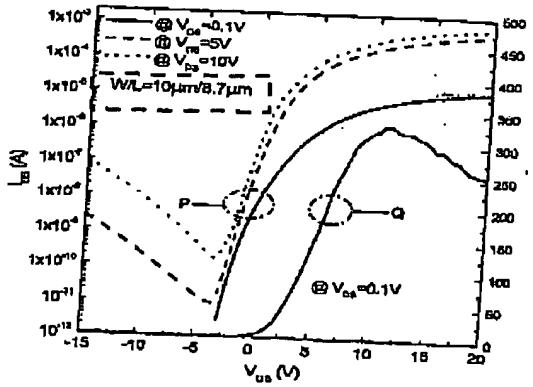


FIG. 6

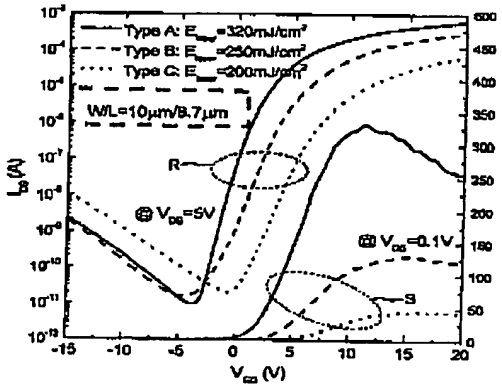


FIG. 7

For at least the foregoing reasons, Applicant respectfully submits that independent claim 1 patently defines over the prior art reference, and should be allowed. For at least the same reasons, dependent claims 2-6 and 8-9 patently define over the prior art as a matter of law, for at least the reason that these dependent claims contain all features of their respective independent claim.

Applicant respectfully traverses the rejection of claim 8 under 35 U.S.C. 103(a) as being unpatentable over Han in view of Sun (U.S. 6,936,848) and claim 9 under 35 U.S.C. 103(a) as being unpatentable over Han in view of Peng (U.S. 6,835,606) because a prima facie case of obviousness has not been established by the Office Action.

Applicants submit that, as disclosed above, Han fails to teach or suggest each and every element of claim 1 from which claims 8 and 9 depend. Sun and Peng also fail to teach or suggest that the width of the gate is smaller than the average grain size of the channel region and the gate does not cross the grain boundary in a direction parallel to the extension direction of the gate. Sun and Peng cannot cure the deficiencies of Han. Therefore, independent claim 1 is patentable over Han, Sun and Peng. For at the least the same reasons, its dependent claims 8 and 9 are also be patentable as a matter of law.

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CONCLUSION

For at least the foregoing reasons, it is believed that the pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Date : June 27, 2006

Respectfully submitted,

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